A 1.9 GHz-BAND ULTRA LOW POWER CONSUMPTION AMPLIFIER CHIP SET FOR PERSONAL COMMUNICATIONS

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Abstract: An ultra low power consumption amplifier chip set for the 1.9 GHz Japanese Personal Handy-phone System (PHS) is presented. The chip set includes a linear power amplifier, a driver amplifier, and an LO switch amplifier. These amplifiers use Cascode FETs that provide low phase distortion, high gain, and low current operation. The power amplifier uses a new concept of a self-phase distortion compensation to achieve a record performance of 45 % power added efficiency with sufficient linearity. The driver amplifier has a gain of 13.5 dB with a low power consumption of 3mW (1mA, 3V). The LO switch amplifier is a new MMIC that has both switch and buffer amplifier functions. The switch amplifier has an output power of 3 dBm, a forward gain of 15 dB, and a reverse isolation of 35 dB with a low power consumption of 6mW (2mA, 3V).

1. Introduction

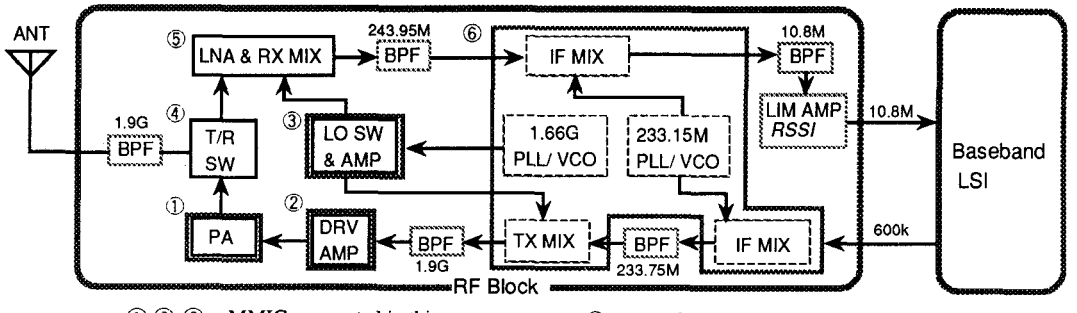
Amplifiers for the 1.9 GHz Japanese Personal Handy-phone System (PHS) requires linear amplification because the system employs narrow-band $\pi/4$-shift QPSK modulation which does not have a constant envelope. Since high efficiency operation is also required for the amplifiers of handy phone sets, especially for the power amplifiers, operation at the near-saturation region is favorable. Many techniques under operation at near-saturation have been proposed for improving linearity [1]. These linearization schemes can be categorized into predistortion, feedforward or feedback techniques. Until now, these techniques have been eagerly investigated to compensate for amplitude distortion, but, as usual, the phase distortion effect has been neglected.

Phase distortion, however, increases significantly through AM/PM conversion at the near-saturation region. Phase distortion, like amplitude distortion, strongly affects the adjacent-channel power-leakage (ACP) and modulation vector error. Therefore, reduction of the phase distortion should be considered. Here, the ACP and modulation vector error specifications of the Japanese PHS standards are -50 dBc at 600 kHz off-carrier and 12.5%rms, respectively.

This paper describes an ultra low power consumption amplifier chip set for the PHS. The chip-set includes a power amplifier, driver amplifier, and LO switch amplifier. These amplifiers provide low power consumption and high linearity simultaneously.

2. RF unit architecture

The 1.9 GHz Japanese PHS employs $\pi/4$-shift QPSK modulation, Time Division Multiple Access (TDMA), and the Time Division Duplex (TDD) scheme. The bit rate and the channel spacing are set at 384 kbps and 300 kHz, respectively. A block diagram of the RF unit for the PHS is shown in Fig. 1. This paper focuses on three new MMICs, which are the power amplifier, driver amplifier, and LO switch amplifier. The T/R switch and low noise amplifier & mixer IC have been reported elsewhere [2]-[4].



①②③ : MMICs presented in this paper.
④ : MMIC reported in Ref. [2].
⑤ : MMIC reported in Refs. [3] and [4].
⑥ : Silicon BiCMOS LSI

Fig. 1 RF unit for Personal Handy Phones.

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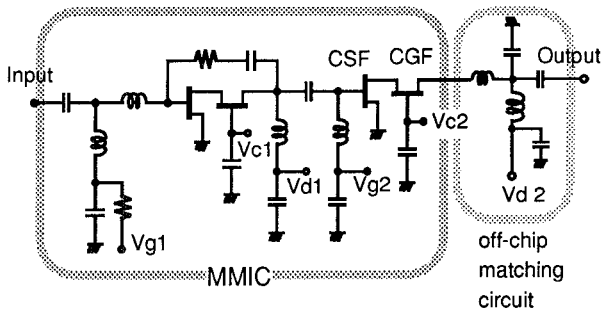
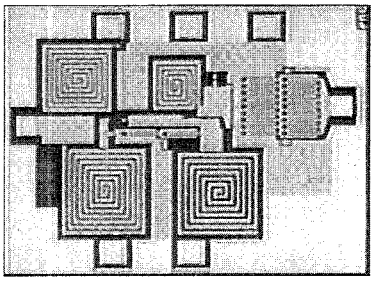
3. Power amplifier

A schematic circuit and a photograph of the new MMIC linear power amplifier are shown in Fig. 2. The amplifier employs a Cascode configuration that is a combination of a common source FET (CSF) and a common gate FET (CGF).. The chip size of the MMIC is 2.0 x 1.5 mm. An off-chip output matching circuit consists of chip inductors and capacitors.

The following facts were uncovered: The output phase deviation of the CSF becomes positive but that of the CGF becomes negative as the input power increases. Therefore, the total output phase deviation of the Cascode FET which is a series combination of the CSF and CGF,





Chip size: 2.0 x 1.5 mm

Fig. 2 Schematic circuit of the power amplifier and a photograph of the MMIC.

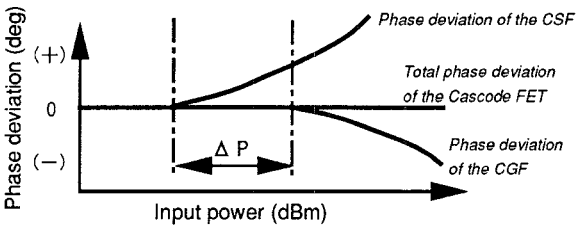


Fig. 3 Self-phase distortion compensation effect of the Cascode FET. (Δ P: Input power level difference caused by gain of the CSF.)

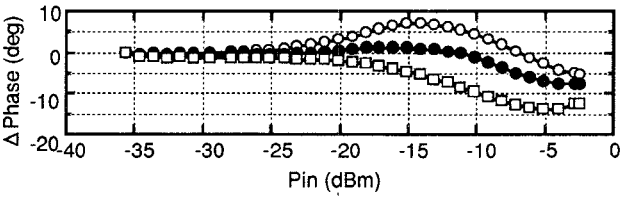
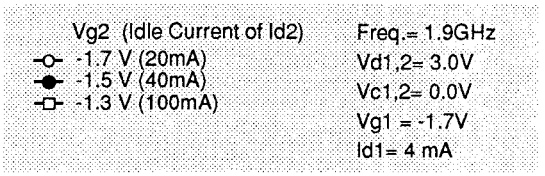


Fig. 4 Output phase deviation versus input power as a function of gate bias Vg2.



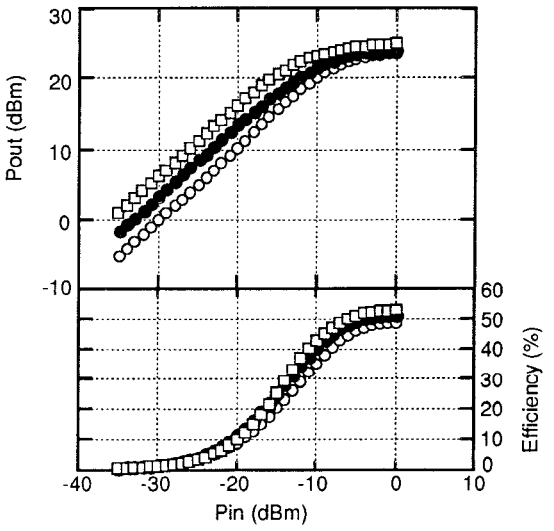


Fig. 5 Output power and power added efficiency versus input power.

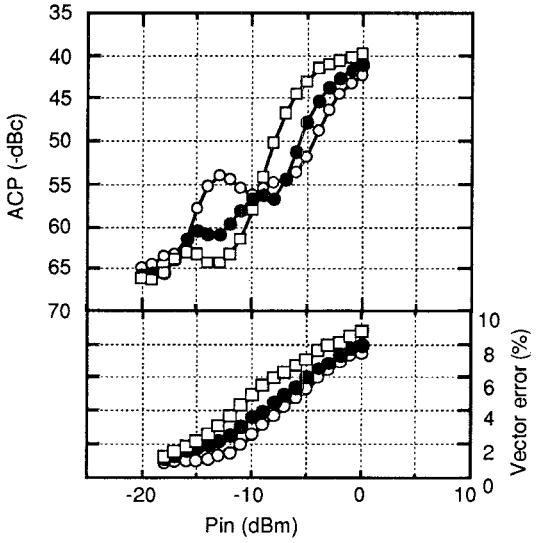


Fig. 6 Adjacent channel leakage and modulation vector error versus input power.

can be reduced at the near-saturation region. We call this effect the self-phase distortion compensation. The effect is caused by the opposite behavior of drain-to-source conductance, Gd, between the CSF and CGF [5]. In order to cancel out the output phase deviation of the Cascode FET, the saturation level of the CGF should be suitably higher than that of the CSF, as shown in Fig. 3, because the input power level of the CGF must be higher from the gain of the CSF. Fortunately, the combination of the saturation levels of the CSF and CGF can be easily changed by adjusting the gate biases because the allotted supplied drain voltage between the CSF and CGS can be controlled by the gate biases [6]. Figure 4 shows measured output phase deviation versus input power as a function of Vg2. The output phase deviations are varied by the gate bias, Vg2, of the CSF. Here, the gate bias,Vc2, of the CGF is a fixed value of 0V. Figure 4 shows that Vg2 of -1.5V is a suitable bias condition for a small output phase deviation and the output phase deviation is only -4 degree at an input power of -8 dBm.

The output power and power-added efficiency versus input power are shown in Fig. 5, and adjacent-channel power-leakage and modulation vector error are shown in Fig. 6. As shown in Fig. 5, a linear gain and a saturated output power are 34dB and 24 dBm at a Vg2 of -1.5V. As shown in Fig. 6, the adjacent-channel power-leakage and modulation vector error are strongly affected by the Vg2 at the near-saturation region (input power of above -15 dBm). At a Vg2 of -1.5V and an input power of -8 dBm, we can obtained good combination of the output power, power added efficiency, ACP, and modulation vector error, i.e., an output power of 22 dBm, a power added efficiency of 45 %, an ACP of -57dBc, and a modulation vector error of 4.3 %rms. This power added efficiency is 5 % higher than the best result of previously reported amplifiers [7]-[10]. Thanks to the self phase distortion compensation effect of the Cascode FET, the amplifier performs sufficiently in spite of the near-saturation operation of 4 dB gain compression. Here, the previously reported amplifiers operated at the 1 dB gain compression point.

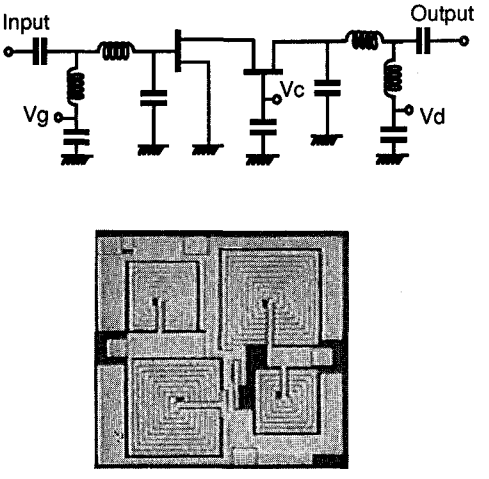
Power amplifier performance is summarized in Table 1.

	RESULT
Output Power	22 dBm
Gain	30 dB
Power Added Efficiency	45 %
ACP @ 600kHz-off	-57 dBc
Modulation Vector Error	4.2 % rms
Vdd / Idd	3.0 V / 116 mA

Table 1 Power amplifier performance. (Pin = -8 dBm)

4. Driver amplifier

The single-stage driver amplifier (DRV) has the same circuit configuration as the power amplifier, as shown in Fig. 7. Since the DRV requires output power of only -8 dBm, a matching design for 1mA operation was applied. The chip size of the DRV is 1.5 x 1.5 mm. DRV performance is summarized in Table 2. A gain of 13.5 dB, an ACP of -65 dBc and a modulation vector error of 1.7 %rms were obtained at 1mA and 3V.



Chip size: 1.5 x 1.5 mm

Fig. 7 Schematic circuit of the driver amplifier and a photograph of the MMIC.

	RESULT
Output Power	-6.5 dBm
Gain	13.5 dB
Power Added Efficiency	6.5 %
ACP @ 600kHz-off	-65 dBc
Modulation Vector Error	1.7 % rms
Vdd / Idd	3.0 V / 1 mA

Table 2 Driver amplifier performance. (Pin = -20dBm)

5. LO switch amplifier

A 1.66 GHz-band first IF local source is supplied to the RX mixer and TX mixer in accordance with the TDD control, as shown in Fig.1. The LO switch amplifier functions as an LO switch and LO buffer amplifier. A schematic circuit of the LO SW amplifier and a photograph are shown in Fig. 8. The chip size is 2.0 x 1.5 mm. The amplifier is essentially based on a Cascode configuration although it consists of one CSF and two CGFs. The two CGFs act as active switches with gain. The circuit is free

from the insertion loss of passive switches and results in low power consumption. The unilateral nature of this circuit is very suitable for an LO buffer amplifier because an LO buffer amplifier requires high reverse isolation in order to stabilize a VCO. Table 3 summarizes the LO switch amplifier performance. The power consumption is only 6mW (2mA, 3V) at a 3dBm output power. The forward and reverse gain are 15 dB and -35 dB, for a difference of 50 dB. This performance is equal to that of a two-stage buffer amplifier.

6. Conclusion

An ultra low power consumption amplifier chip set for the 1.9 GHz Japanese Personal Handy-phone System (PHS) have been described. The amplifiers use Cascode FETs that provide low phase distortion, high gain and low current operation. Thanks to the self-phase distortion compensation effect of Cascode FETs, the power amplifier performs well in spite of the near-saturation operation of 4-dB gain compression. The power amplifier achieves a record performance of 45 % power added efficiency, which is 5 % higher than the best result for previously reported amplifiers.

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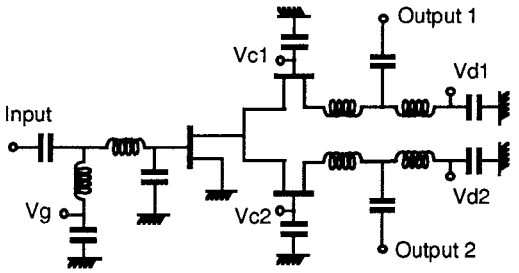

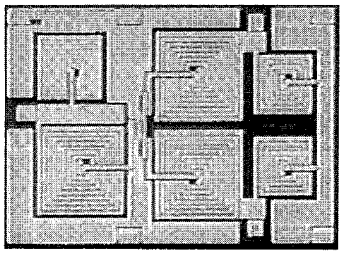

Chip size: 2.0 x 1.5 mm

Fig. 8 Schematic circuit of the LO switch amplifier and a photograph of the MMIC.

References

[1] K. Chiba, T. Nojima, and S. Tomisato, "Linearized saturation amplifier with bidirectional control for digital mobile radio," *in Proc. of IEEE Globecomm., pp. 1958-1962, 1990.*

[2] T. Tokumitsu, I. Toyoda, and M. Aikawa, "Low voltage, high power T/R switch MMIC using LC resonators," *IEEE 1993 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, pp. 27-30, June 1993.*

[3] M. Nakatsugawa, Y. Yamaguchi, and M. Muraguchi, "An L-band ultra low power consumption monolithic low noise amplifier," *IEEE GaAs IC Symp. Tech. Digest, pp. 45-48, Oct. 1993.*

[4] Y. Yamaguchi, A. Minakawa, M. Nakatsugawa, and M. Muraguchi, "A very low power L-band front-end MMIC," *The Fourth International Symposium on Personal, Indoor and Mobile Radio Communications Digest, pp. 412-415, Sept. 1993.*

[5] H. Hayashi, M. Nakatsugawa, and M. Muraguchi, "Quasi-linear amplification using self phase distortion compensation technique," *submitted to IEEE Trans. Microwave Theory Tech.*

[6] M. Muraguchi, M. Nakatsugawa, and M. Aikawa, "A novel MMIC power amplifier for pocket-size cellular telephones," *IEEE MTT-S Int. Microwave Symp. Digest, pp. 793-796, June 1993.*

[7] S. Makioka, K. Tateoka, M. Yuri, N. Yoshikawa, and K. Kanazawa, "A high efficiency GaAs MCM power amplifier for 1.9GHz digital cordless telephones," *IEEE 1994 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, pp. 51-54, June 1994.*

[8] T. Kunihisa, T. Yokoyama, H. Fujimoto, K. Ishida, H. Takehara, and O. Ishikawa , "High efficiency, low adjacent channel leakage GaAs power MMIC for digital cordless telephones," *IEEE 1994 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, pp. 55-58, June 1994.*

[9] T. Yoshimasu, N. Tanba and S. Hara , "An HBT MMIC linear power amplifier for 1.9 GHz personal communications," *IEEE 1994 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, pp. 59-62, June 1994.*

[10] M. Nagaoka, el al., "High-efficiency monolithic GaAs power MESFET amplifier operating with a single low voltage supply for 1.9-GHz digital mobile communication applications," *IEEE MTT-S Int. Microwave Symp. Digest, pp. 577-580, June 1994.*

		RESULT
GAIN	IN to OUT(on)	15 dB
	IN to OUT(off)	-35 dB
ISOLATION	OUT(on) to IN	35 dB
	OUT(off) to IN	35 dB
	OUT(on) to OUT (off)	40 dB
	OUT(off) to OUT (on)	20 dB
INPUT RETURN LOSS		15 dB
OUTPUT RETURN LOSS ON PORT / OFF PORT		9 dB / 8 dB
Vdd / Idd		3 V / 2 mA

Table 3 LO switch amplifier performance.